Electronic Version

Stylesheet Version v1.1.1

Claims

[c1] 1.A parallel tester for testing a panel of memory modules comprising:

a plurality of upper test heads, each upper test head having pad contactors for making electrical contact with metal pads on one of the memory modules on the panel of memory modules;

a plurality of lower test heads, each lower test head hav-ing pad contactors for making electrical contact with metal pads on the memory module on the panel of memory modules;

a plurality of test drivers for applying test signals to the upper and lower test heads, the test signals for applying test conditions to the memory modules through the pad contactors and the metal pads, each test driver sensing current or voltage conditions on at least one of the metal pads and comparing the current or voltage conditions to predetermined conditions to determine when the mem-ory module has failed; and

a positioner that handles the panel and moves the panel into a test position between the upper and lower test heads and removes the panel from the test position after testing by the test driver;

wherein the upper test heads are lowered relative to the panel in the test position, and the lower test heads are raised relative to the panel in the test position, to make contact with the metal pads on upper and lower surfaces of a plurality of the memory modules on the panel;
wherein the plurality of memory modules on the panel are tested in parallel.

[c2] 2.The parallel tester of claim 1 wherein the plurality of upper test heads comprises one test head and set of pad contactors for each memory module on the panel;
wherein the plurality of lower test heads comprises one test head and set of pad contactors for each memory module on the panel;
wherein the plurality of test drivers comprises one test driver for each memory module on the panel,
whereby all memory modules on the panel are tested in parallel.

[c3] 3.The parallel tester of claim 2 further comprising:
a marker, responsive to the plurality of test drivers, for marking memory modules on the panel that the plurality of test drivers have indicated as failures,
whereby failing memory modules are marked.

[c4] 4.The parallel tester of claim 3 wherein the marker is an inker that applies a drop of ink to failing memory mod-

ules on a panel to mark failing memory modules.

[c5] 5.The parallel tester of claim 1 wherein the panel further comprises panel links that link the memory modules together as a single panel;
wherein the positioner handles the panel by panel links;
wherein the pad contactors do not contact the panel on the panel links.

[c6] 6.The parallel tester of claim 5 wherein the positioner comprises a conveyer system that holds the panel by the panel links, a robotic arm that grips the panel by the panel links, or a handler that guides the panel by the panel links.

[c7] 7.The parallel tester of claim 6 wherein the test signals from the plurality of test drivers activate memory chips mounted on the memory modules,
whereby the memory chips on the memory modules are tested.

[c8] 8.The parallel tester of claim 7 wherein the pad contactors comprise pins, metal bumps, or spring-loaded pins.

[c9] 9.A panel tester comprising:
first means for making electrical contact with contact pads on a first surface of a memory module that is part of a panel of a plurality of memory modules before sep-

aration;

second means for making electrical contact with contact pads on a second surface of the memory module that is part of the panel of memory modules before separation;

placement means for moving the panel into a test position where the first means and the second means can both make electrical contact with the contact pads of the memory module;

test driver means, coupled to the first and second means, for driving test signals to the contact pads and for sensing test conditions from the contact pads and detecting a failure of the memory module; and

indicating means, coupled to the test driver means, for indicating when the memory module has failed,

whereby the memory module that is part of the panel of the plurality of memory modules before separation is tested before separation from the panel.

[c10] 10.The panel tester of claim 9 wherein the first means includes a plurality of first head means, each first head means for making electrical contact with contact pads on the first surface of a different one of the plurality of memory modules on the panel;

wherein the second means includes a plurality of second head means, each second head means for making electrical contact with contact pads on the second surface of

a different one of the plurality of memory modules on the panel;

wherein the test driver means drives the test signals to the plurality of first and second head means to test several of the memory modules on the panel;

wherein the indicating means indicates which of the plurality of memory modules has failed,

whereby several memory modules on the panel are tested simultaneously.

[c11] 11.The panel tester of claim 10 wherein the indicating means marks memory modules on the panel that have failed, but does not mark memory modules on the panel that have not failed.

[c12] 12.The panel tester of claim 9 further comprising:

first pitch means, coupled to the plurality of first head means, for setting a pitch of the plurality of first head means to match a pitch between contact pads from one memory module to another memory module on the panel;

second pitch means, coupled to the plurality of second head means, for setting a pitch of the plurality of second head means to match the pitch between contact pads from one memory module to another memory module on the panel,

whereby panels having different spacing of memory

modules can be tested by adjusting the panel tester.